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Research Paper

# Design and development of Low Noise Amplifier for RF/MW Receiver

Engineering

**KEYWORDS :** HEMT, Noise Figure, Wideband LNA, AWR

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## ABSTRACT

*LNA design is a crucial thing and challenging task at the receiver since received signal will always be weaker in amplitude and corrupted by noise in wireless communications. It should provide low noise figure not only at one frequency but over range of frequencies or bandwidth of interest. Also requirements of minimum noise figure and maximum gain will always be design trade-offs and can't be met simultaneously. We need an optimization and fine tuning of component values to get the optimum results. For radio astronomy applications, it's desirable to have wider bandwidth, low noise figure and good gain. Sometimes we need to sacrifice gain for bandwidth. High electron mobility transistor (HEMT) plays a crucial role and is extensively used in ultra low noise amplifiers. We have designed two stage LNA at the centre frequency of 1.5GHz and achieved bandwidth of around 1.2GHz while maintaining noise figure of 0.54 dB, unconditional stability and gain of 25dB using AWR Microwave Office software.*

### I. INTRODUCTION
A low noise amplifier (LNA) is a device used in communication systems which amplifies very weak signals captured by the antenna. Almost in any communication device, the LNA is located very close to the receiving antenna; in fact, the first component after the antenna is the low noise amplifier.LNA should boost desired signal power while adding as little noise and distortion as possible [8]. An LNA is the combination of low noise, high gain and stability over the entire range of operating frequency. Wireless communications are very lossy, so signals travelling from far away normally suffer from a lot of degradation. When these signals are received at the antenna, they are very weak, that is why the LNA is used very close to the antenna. Also losses in the feed line become less critical if LNA is located very close to the antenna.

The received signal is typically filtered, amplified by an LNA and translated to the base-band by mixing with a local-oscillator. After being demodulated, the signal is applied to an Analog-to-Digital converter (ADC) which digitizes the analog signal. The digital signal is then processed in a Digital Signal Processing unit (DSP).

In astronomy, the sensitivity of the radio Telescope i.e., the ability to detect very weak signals coming from the radio emissions, depends on the area and efficiency of the antenna. And the sensitivity of the radio receiver is used to detect and amplify weak signals coming from the radio sources. So a noise figure is the most important parameter in radio telescope as the sensitivity depends on its value, the smaller it is, the higher is the sensitivity of the telescope [9].

### II. TECHNICAL SPECIFICATIONS
Wideband LNA design Specifications:

- Operating frequency range -1 to 3 GHz
- Noise figure - 0.2 to 0.4dB (as it should be as low as possible)
- Gain >20dB or 30 dB
- Input and output VSWR – In between 1 to 2
- Bandwidth – 1 to 2GHz

### III. DESIGN CONCEPT
While designing LNA in general we need to consider following important parameters out of which suitable component (active device) selection is the first vital step. We must keep in mind the trade-offs between various key parameters while designing. S-parameters and noise figure parameters are required to characterize the device [1]-[3].

Key design parameters to be considered for LNA are,

- Desired noise figure (in dB)
- Gain and gain flatness (in dB)
- Operating frequency and Bandwidth (in Hz)
- Input and output reflection coefficients (or VSWR)
- Proper biasing conditions (passive or active biasing)
- Selection of proper transistor (first important step)
- Amplifier's stability (K>1, |Δ|<1)
- Third order intercept point (TOIP) (in dBm)
- Good sensitivity is desirable
- Good linearity
- Good dynamic range (for astronomy applications)

Based on the amplifier's specifications and application we have to select an appropriate device. We need to apply suitable DC bias for proper functioning of the transistor. Input and output matching networks can be designed by either transmission line sections or reactive components or combination of both. Fig.1 illustrates the basic block diagram of LNA.

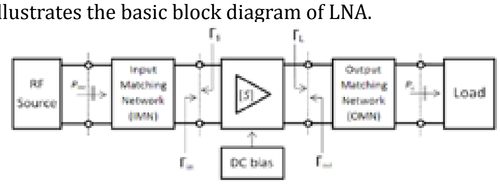


**Fig. 1 Generalized block diagram of LNA design [2]**

#### A. Device Selection
Active device selection is the first vital step in LNA design. The designer should carefully review the transistor selection keeping the most important design tradeoffs in mind. Examination of the data sheet is a good starting point in the transistor evaluation for LNA design. We have selected ATF 35143 pHEMT which is a depletion mode device.

#### B. Stability Check and Enhancement
Stability of the circuit is nothing but it's resistance to oscillations. Stability is an indispensible part of LNA. Unconditional stability is the goal of the designer. It means that for any source and load impedance the circuit should not oscillate. Otherwise proper techniques are applied to make it stable for given frequency range. S-parameters play a vital role in stability analysis.

**1) Analytical solution of stability criteria:**
Two parameter test (K>1, |Δ|<1) where

$$K = [1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2] / [2 |S_{12}| |S_{21}|]$$

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and $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$

Single parameter test ($\mu>1$), $\mu_A>\mu_B$, Device A more stable [1]

**2) Graphical solution of stability criteria:**
Smith chart is used to plot of input and output stability circles for conditional stability ($|\Gamma_{IN}| >1$ and $|\Gamma_{OUT}| >1$ where

$\Gamma_{IN} = S_{11}+ [(S_{12} S_{21} \Gamma_L) / (1- S_{22} \Gamma_L)]$ and

$\Gamma_{OUT} = S_{22}+ [(S_{12} S_{21} \Gamma_S) / (1- S_{11} \Gamma_s)]$

**3) Stability Enhancement:**
There are different techniques to enhance the stability. Some of them are listed below.

**(a) Adding a series resistance:**
A small resistance is added in series or shunt with the drain of the transistor. This will increase the noise figure of the amplifier. It's preferable not to use any noisy component.

**(b)Use of source inductance (inductive degeneration):**
Another method of improving stability is to add an inductor to the source leg. A source inductor acts like a noise less resistance. But this reduces gain by a small factor. The additional inductance between the source and ground provides lossless negative series feedback. An added benefit arising from the use of the source inductance is that the input conjugate match, $\Gamma_{11}^*$, is moved closer to the optimal noise match, $\Gamma_{opt}$.

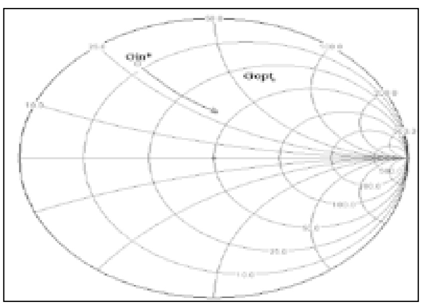

**Fig. 2 Additional source inductance shifts the conjugate match closer to the optimal noise match [7]**

**C. Biasing of the Device**
DC biasing network is required to provide stable operating point for the device. Biasing circuit must be protected from the high frequency effects. For that purpose RFC and blocking capacitors are useful. We have used passive biasing due to it's simplicity and selected $V_{DS}$=2V, $I_D$=10mA with –ve $V_{GS}$. So we require dual power supply.

$$V_{GS} = V_P (1 - \sqrt{Id/Idss})$$

*D. Noise Figure Considerations*
The lower the noise figure, the better the LNA as it means less noise is added by the LNA. In telecommunications, noise factor is the measurement of degradation of signal to noise ratio.

Noise figure (F) = 10 log $[(S/N)_{in} / (S/N)_{out}]$
In generalized form,
$F= F_{min}+ (R_n / G_s) |Y_s-Y_{opt}|^2$
For two stage cascade,
$F = F_1 + (F_2-1)/G_{A1}$ or $T_e= T_{e1} + (T_{e2} /G_{A1})$

So first stage N.F. and gain has a large influence on overall N.F. or noise temperature. So the key to low overall N.F. is to focus on first stage by reducing it's noise and increasing it's gain. Later stages have greatly reduced effect on the overall N.F.

*E. Gain Considerations*
Gain of the amplifier is the ratio of output power to input power. For LNA design there are three power gain definitions appears in the literature.

- Transducer power gain (GT)
- Operating power gain (GP)
- Available power gain (GA)

*F. Impedance Matching*
Input and output matching networks transition the device to the outside world. Basic objective of matching network is not only to transfer maximum power but also to improve SNR [1].

To have a best compromise between gain and N.F., lossless matching networks (ideally) must be designed to transform the input and output impedance to source and load impedances required in the design specifications. Inter stage matching networks are required in case of cascading. The losses of the matching networks are related to the Q of the components and associated printed circuit board loss.

Input matching network at the input side should give minimum noise matching principle and output matching network is required for maximum gain matching principle and its flatness [5].

That is, $\Gamma_S= \Gamma_{opt}$ to get $F=F_{min}$ for simultaneous i/p and noise matching and $\Gamma_L = \Gamma_{out}^*$ or $ZL = Z_{out}^*$.

**IV. FLOWCHART**


**Fig. 3 Generalized flowchart of LNA design**

**V. DESIGN AND SIMULATION IN AWR**
It is found that the selected ATF 35143 is unstable in the desired frequency range. We can verify this in AWR using stability circles as shown in Fig.4. Usually at low frequency, FET is potentially unstable without the addition of Ls and some resistive element. As the source lead inductance is increased, the stability factor increases rapidly. So we have added extra resistor at the drain side to get unconditional stability throughout the frequency range of interest. Fig. 4 shows unstable regions on the smith chart.

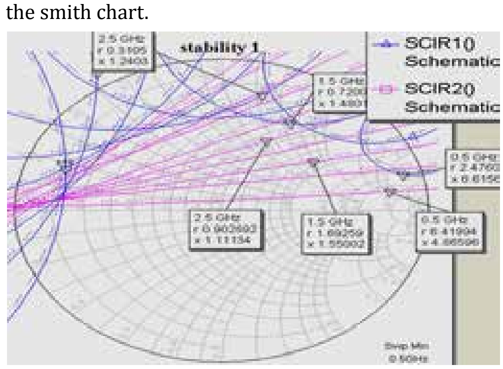


**Fig. 4 Stability check for the device in AWR**

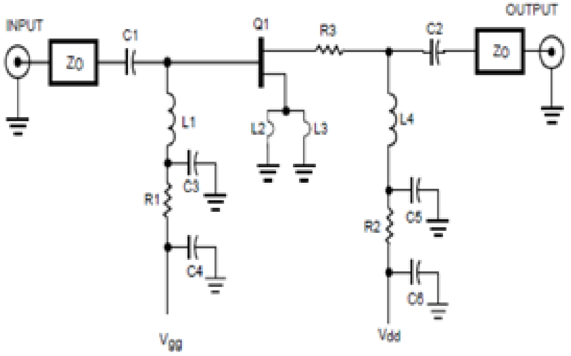


**Fig. 5 Circuit diagram for single stage LNA [6]**

As shown in Fig.5, the amplifier uses a high-pass impedance matching network for input noise match and output conjugate match. The high pass network consists of a series capacitor and a shunt inductor. The L-section matching networks also double as a means of inserting gate and drain voltages for biasing. Additionally, the series capacitors C1 and C2 also function as DC blocking capacitors. L1 also doubles as a means of inserting gate voltage for biasing up the pHEMT. This requires a good bypass capacitor in the form of C3.

The Q of L1 is also extremely important from the standpoint of circuit loss which directly relates to noise figure. Resistor R3 and capacitors C3, C5 provide in-band stability, while resistors R1 and R2 provide low frequency stability by providing a resistive termination. The resistive loading, R3, is one of the main contributors to stability along with the inductance in the ground path. C4, C6 performs low frequency bypassing. Also extra capacitor may be needed to minimize power supply noise from modulating the DC. Increasing L2, L3 reduces gain and improves input-IP3, but we must watch for microwave oscillation with excessive source inductance [6].

Figures 6, 7 and 8 as shown below represents single stage LNA design using real components and simulated results in AWR microwave office software.

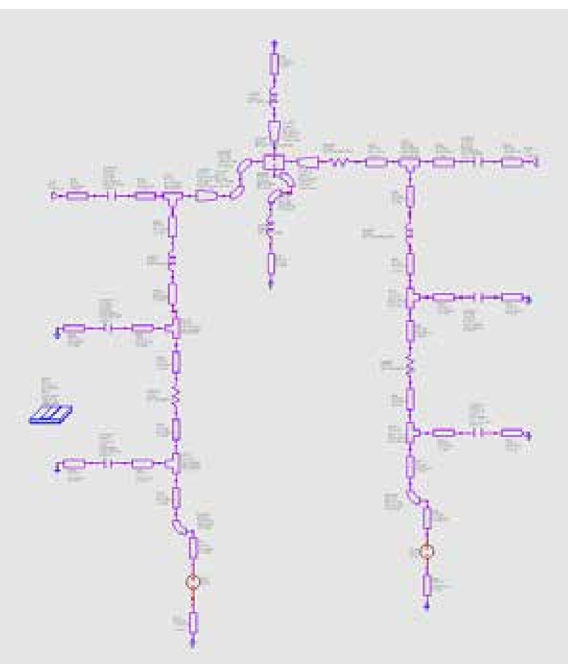

**Fig. 6 Single stage design with real components and transmission lines**

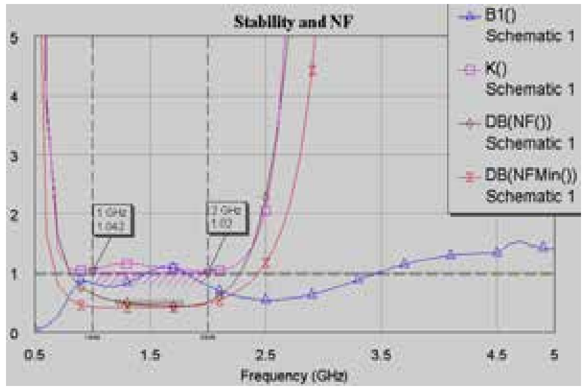


**Fig.7 Stability and noise figure of single stage LNA**

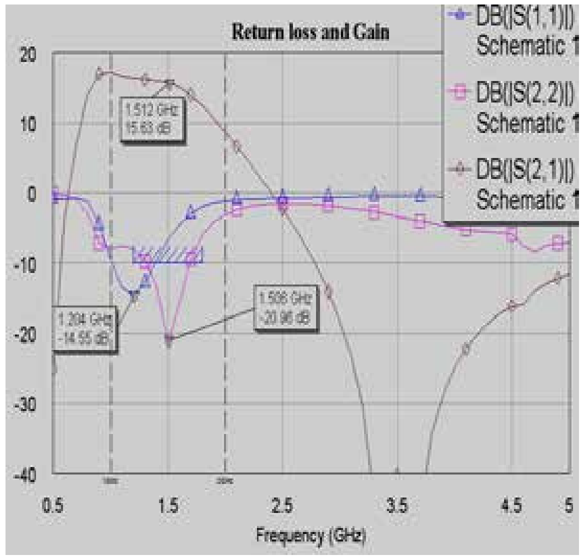


**Fig. 8 Gain and return loss of single stage LNA**

In the similar way we have designed two stage LNA by incorporating inter stage matching network between two transistors. The topology uses two amplifiers and it is an extension of single stage. It gives more gain and stability than single stage. Also we have observed the improvement in the input and output return loss bandwidth due to greater amount of flexibility in tuning for matching networks.Fig.9 and Fig.10 depicts two stage LNA simulated results.

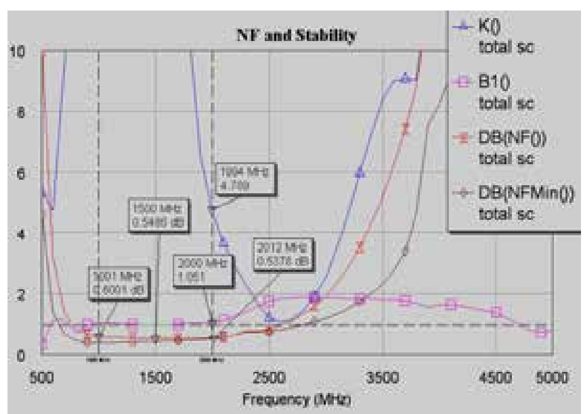


**Fig.9 Stability and noise figure of two stage LNA**

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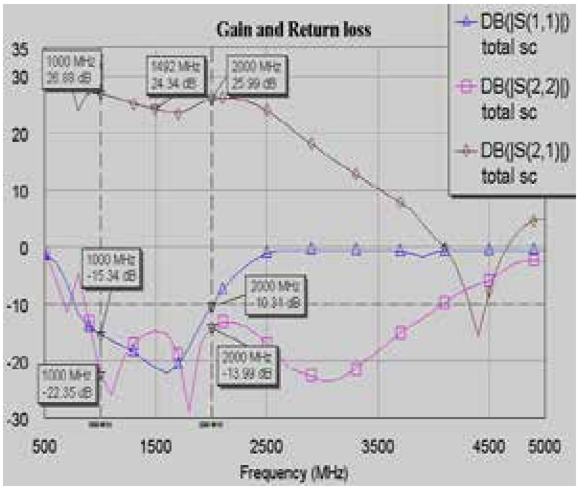



**Fig.10 Gain and return loss of two stage LNA**

### VI. COMPARISON OF 1STAGE AND 2STAGE LNA

Following Table1 gives comparison of both the stages.

**TABLE I COMPARISON OF 1STAGE AND 2STAGE LNA**

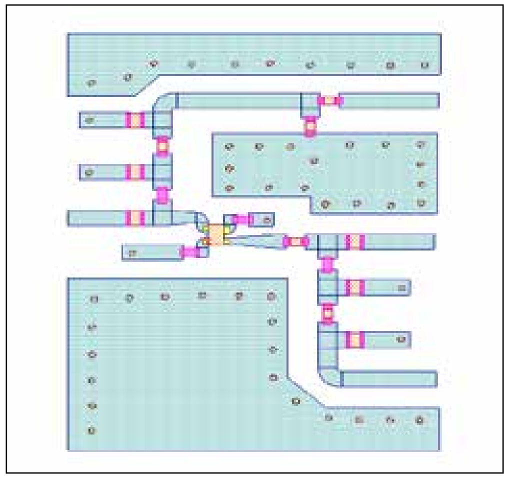
| Parameter | Single stage LNA | Double stage LNA |
|---|---|---|
| Stability (K and β) | K>1 and β1 throughout 500Mhz to 5GHz | K>1 and β1 throughout 500Mhz to 5GHz |
| Noise Figure(in dB) | 0.45 to 0.6 dB from 1 to 2 GHz | 0.54 to 0.58 dB from 1 to 2 GHz |
| Gain ($S_{21}$ in dB) | 17dB to 9dB from 1 to 2GHz | 24 to 27 dB from 800Mhz to 2.5GHz |
| Return loss($S_{11}$ and $S_{22}$ in dB) | $S_{11}$< -10dB from 1 to 1.4GHz (BW 400MHz) $S_{22}$< -10dB from 1.3 to 1.7 GHz (BW 400MHz) | $S_{11}$< -10dB from 750MHz to 2 GHz (BW > 1GHz) $S_{22}$< -10dB from 860MHz to 4 GHz (BW 3GHz) |

### VII. LAYOUT AND FABRICATION OF LNA

Layout is the view of the physical representation of a schematic. Layout is a critical part of high frequency circuit design and simulation, since the response of the circuit is dependent on the geometric shapes with which it's composed. The first step in fabrication of the LNA is generating the layout from the schematic. For creating a layout of the design, all the wires are removed and the lumped components and devices are connected using the microstrip lines. If there is a node where three circuit paths are being combined, it can be replaced by a MTEE microstrip line. To make a connection between the two components on the circuit path ,MLIN microstrip line can be used. To make a layout for any RF circuits the designer needs a real component foot prints. For this task, real components from Coilcraft, TOKO, ATC, Panasonic are chosen.

During the fabrication process, Plating Through Hole (PTH) requirement arises when grounding the source of the device. There is ground on one side of the substrate and circuit lies on the other, in between the two is a dielectric.Fig.11 and Fig.12 represents layout of both stages along with real component footprints and PTH.

**Fig.11 Layout of single stage LNA**



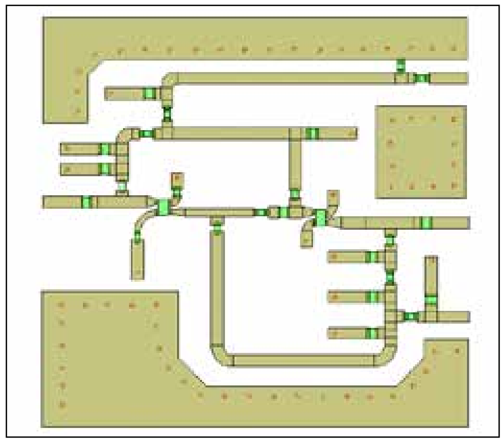


**Fig.12 Layout of two stage LNA**

### VIII. CONCLUSION

In LNA design, the designer's first goal is to achieve the unconditional stability over the complete range of frequencies along with substantial gain and low noise figure which we have achieved for both stages in AWR simulation. Source inductance acts as a series negative feedback which helps to improve input VSWR and low noise by reducing the gain. Extra series resistance at the drain of the transistor is added for unconditional stability. So NF and gain are sacrificed. For two stage, mismatch at the output of the first-stage can then be optimized to improve input return loss without adversely effecting noise figure. Testing and measurement is yet to be completed.

### ACKNOWLEDGMENT

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