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FPGA IMPLEMENTATION OF HIGH SPEED PIPELINED DDRSDRAM MEMORY CONTROLLER

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ABSTRACT In real time applications Double Data Rate Synchronous DRAM (DDR SDRAM) became mainstream choice in designing memories due to its burst access, speed and pipeline features. Synchronous dynamic access memory is designed to support DDR transferring. To achieve the correctness of different applications and system work as to be intended, the memory controller must be configured with pipelined design for multiple operations without delay. However, for other applications, the system designer must design a controller to provide proper commands for SDRAM initialization, read/write accesses and memory refresh. DDR SDRAM uses double data rate architecture to achieve high-speed data transfers. Double data rate is, the data is transferred on every rising edge and every falling edge of the clock as a result the throughput is increased. here the data is transferred in first in first out operation. In this the controller is acts as an interface between bus master and DDRSDRAM.The data is transferred through the buses. In the proposed paper DDRSDRAM controller is designing using the pipelining process. In the pipelining process instructions executed in parallelism and speed is increased. the paper is designed in field programmable gate arrays. Here the data is reprogrammable and reusable. We are designing our architecture in Verilog HDL code using Vivado 14.3 and implemented on Zynq Board(FPGA).

KEYWORDS : Synchronous DRAM, Column Access Strobe, Row Access Strobe,FPGA.

INTRODUCTION

Memory devices are almost found in all systems and nowadays high speed and high performance memories are in great demand. For better throughput and speed, the controllers are to be designed with clock frequency in the range of megahertz. As the clock speed of the controller is increasing, the design challenges are also becoming complex. Therefore the next generation memory devices require very high speed controllers like double data rate and quad data rate memory controllers. In this paper, the double data rate SDRAM Controller is implemented using FPGA methodology. In this paper, the SDRAM controller, located between the SDRAM and the bus master, minimizes the effort to deal with the SDRAM memory by providing a simple system to interact with the bus master. Figure 1 is the block diagram of the DDR SDRAM Memory Controller that is connected between the bus master and SDRAM .SDRAM's are classified based on their data transfer rates. In Single data rate SDRAM, the data is transferred on every rising edge of the clock whereas in double data rate (DDR) SDRAM's the data is transferred on every rising edge and every falling edge of the clock and as a result the throughput is increased. DDR SDRAM Controllers are faster and efficient than its counterparts. They allow data transfer at a faster rate without much increase in clock frequency and bus width.

Double Data Rate Synchronous Dynamic Random Access Memory is the original form of DDR SDRAM. It is just like SDRAM except that is has higher bandwidth, meaning greater speed. Maximum transfer rate to L2 cache is approximately 1,064 Mbps (for DDR SDRAM 133 MHZ).

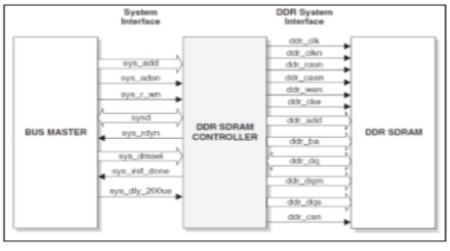


Fig1.DDRSDRAM controller system

DDR RAM is clock doubled version of SDRAM, which is replacing SDRAM during 2001 2002. Allows transactions on both the rising and falling edges of the clock cycle. It has a bus clock speed of 100MHz and will yield an effective data transfer rate of 200MHz. DDR come in PC 1600, PC 2100, PC 2700 and PC 3200 DIMMs. A PC 1600 DIMM is made up of PC 200 DDR chips, while a PC 2100 DIMM is made up of PC 266 chips. Go for PC2700 DDR. It is about the cost of PC2100 memory and will give you better performance. DDR memory comes in CAS 2 and CAS 2.5 ratings, with CAS 2 costing more and performing better.

DESCRIPTION

DDR SDRAM Controller module receives addresses and control signals from the BUS Master. The Controller generates command signals and based on these signals the data is either read or written to a particular memory location. The DDR SDRAM Controller architecture is shown in Figure 2. It consists of three modules: 1) Main control module 2) signal generation module 3) data path module. 1.The main control module has two state machines and a refresh counter. The two state machines are for initialization of the SDRAM and for generating the commands to the SDRAM. They generate iState and cState outputs according to the system interface control signals. The signal generation module now generates the address and command signals depending upon the iState and cState. The data path module performs the read and write operations between the bus master and DDR.

The main control module consists of three sub modules: 1)Initialization FSM module (INIT_FSM). 2)Command FSM module (CMD_FSM) 3) Counter module.

Following are some of the important features of DDR SDRAM Controller:

i. The DDR SDRAM Read and Write operations are simplified by the controller.
ii. The access time for read and the write cycle is optimized based on the CAS latency and burst length of the DDR SDRAM.
iii. For initializing the DDR SDRAM controller, separate state machines are designed internally.

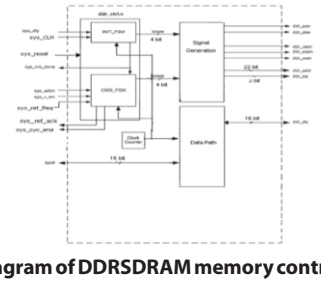


Fig2.Block diagram of DDRSDRAM memory controller

1.Main control module:

1.DDR SDRAM initial fsm:

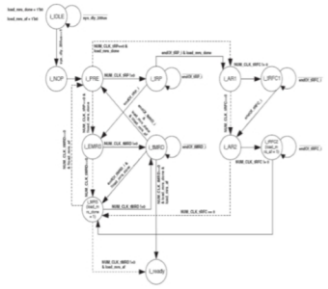


Fig3.FSM diagram for initial state

i. Different states of Initial FSM:

Idle: When reset is applied the initial fsm is forced to IDLE state irrespective of which state it is actually in when system is in idle it remains idle without performing any operations.

No Operation (NOP): The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Precharge (PRE): The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The value on the BA0, BA1 inputs selects the bank, and the A10 input selects whether a single bank is precharged or whether all banks are precharged.

Auto Refresh (AR): AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-before-RAS# (CBR) refresh in DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

Load Mode Register (LMR): The mode registers are loaded via inputs A0–An. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

Read/Write Cycle: The state diagram of CMD_FSM which handles the read, write and refresh of the SDRAM. The CMD_FSM state machine is initialized to c_idle during reset.After reset, CMD_FSM stays in c_idle as long as sys_INIT_DONE is low which indicates the SDRAM initialization sequence is not yet completed.

Once the initialization is done, sys_ADSn and sys_REF_REQ will be sampled at the rising edge of every clock cycle. A logic high sampled on sys_REF_REQ will start a SDRAM refresh cycle. This is described in the following section. If logic low is sampled on both sys_REF_REQ and sys_ADSn, a system read cycle or system write cycle will begin. These system cycles are made up of a sequence of SDRAM commands.

2.DDR SDRAM command fsm:

Fig4.FSM for Command state

I. Different states of Command FSM:

Refresh Cycle: DDR memory needs a periodic refresh to hold the data. This periodic refresh is done using AUTO REFRESH command. All banks must be idle before an AUTO REFRESH command is issued. In this design all banks will be in idle state, as every read/write operation uses auto pre charge.

Active (ACT): The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access, like a read or a write.The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–An selects the row.

Read: The READ command is used to initiate a burst read access to an active row, as shown in Figure. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where Ai is the most significant column address bit for a given density and configuration) selects the starting column location.

Write: The WRITE command is used to initiate a burst write access to an active row as shown in Figure.The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where Ai is the most significant column address bit for a given density and configuration) selects the starting column location.

Refresh Cycle: Similar to the other DRAMs, memory refresh is required. A SDRAM refresh request is generated by activating sdr_REF_REQ signal of the controller. The sdr_REF_ACK signal will acknowledge the recognition of sdr_REF_REQ and will be active throughout the whole refresh cycle. The sdr_REF_REQ signal must be maintained until the sdr_REF_ACK goes active in order to be recognized as a refresh cycle. Note that no system read/write access cycles are allowed when sdr_REF_ACK is active. All system interface cycles will be ignored during this period. The sdr_REF_REQ signal assertion needs to be removed upon receipt of sdr_REF_ACK acknowledge, otherwise another refresh cycle will again be performed.

Upon receipt of sdr_REF_REQ assertion, the state machine CMD_FSM enters the c_AR state to issue an AUTO REFRESH command to the SDRAM. After tRFC time delay is satisfied, CMD_FSM returns to c_idle.

Pipelined DDRSDRAM state fsm :

Fig5.Pipelined fsm

In pipelined version we can perform multi operations like read and write in different memory locations simultaneously.

2.Signal generation module:

The signal generation module with inputs and outputs as shown in the figure. The signal generation module generates the address and command signals required for DDRSDRAM.

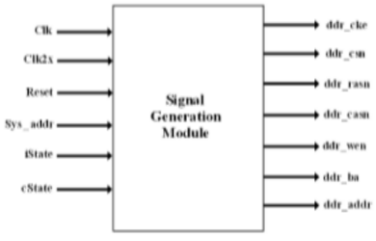


Fig6.signal generation module

The command signals include ddr_add; for generating addresses, ddr_casn and ddr_rasn; for selecting particular column and row address. These signals are generated based on the iState and cState received from the CMD_FSM and INIT_FSM present in the Main Control module.

3. Datapath module:

The data flow design between the SDRAM and the system interface. The DDR SDRAM Controller design interfaces between the 16-bit data bus, and the bus master with a 16-bit data bus.

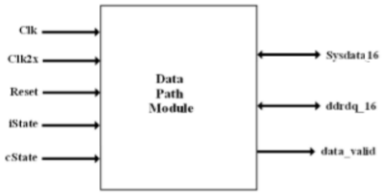


Fig7.datapath module

The data path module for read and write operation. The data path module depends on cState for its read/write operation. The cState is generated by the CMD_FSM present in the Main Control module.The data path module performs the data latching and dispatching of the data between the processor and DDR.

FEATURES:

- The DDR SDRAM Read and Write operations are simplified by the controller.
- For initializing the DDR SDRAM controller, separate state machines are designed internally.
- The access time for read and the write cycle is optimized based on the CAS latency and burst length of the DDR SDRAM.
- The auto refresh for the DDR SDRAM is done by the controller.

We are designing our architecture in Verilog HDL code using Vivado 14.3 and implemented on Zynq Board .The below section will give brief introduction about Verilog HDL and Vivado Design Suite.

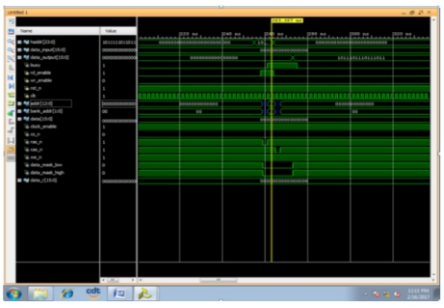
TEST RESULTS

COMPARISION TABLE:

In the base paper frequency=186.881mhz, speed=30ns.

COMPONENT	BASE PAPER	PROPOSED
Speed (ns)	30	31.2
Counters	6	2
Registers	150	98
Power (mW)	15.86	12

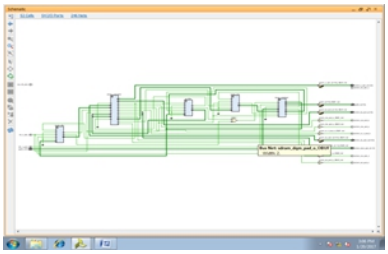
SIMULATION WAVEFORM:



If clk=1,reset=1,the operation will be in busy state.

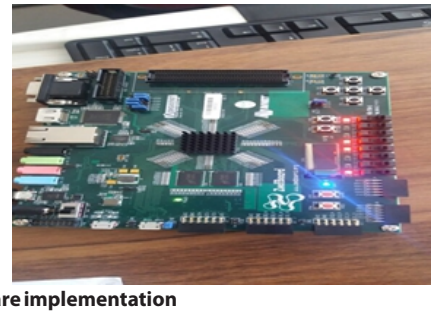
If clk=1,reset=0 any one(read/write)operation performed.

SCHEMATIC OF DDRSDRAM MEMORY CONTROLLER:



HARDWARE IMPLEMENTATION

Hardware implementation
when reset=1, read=0,write=1 then dout=0



Hardware implementation
when reset=0,read=1,write=1 then din=dout=10011001

CONCLUSION

FPGA Design methodology is opted for Double Data Rate (DDR) SDRAM Controller. The DDR SDRAM Controller architecture is implemented in Verilog HDL by using Xilinx Vivado IDE Tool can conclude that speed can be improved by using pipelining technique and time delay is reduced. In future this design can be implemented for DDR2/DDR3 also. This is one of the efficient designs for pipeline the memory accessing and multiple operations without including the much delay.

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