Original Research Paper Engineering

FPGA IMPLEMENTATION OF AN EFFICIENT TPG

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ABSTRACT The main focus of this paper is to generate multiple test patterns. The test patterns which are generated by Linear feedback shift register and is lack of correlation between the subsequent test patterns. In order to overcome this drawback of LFSR we are generating the test patterns by Gray counter and Decoder. By generating the test patterns with Gray counter and decoder the Area reduction 30% is achieved i.e by reducing the total gate count.TPG using gray counter and decoder is coded by using Verilog ,Simulations and Synthesis are performed by Xilinx Vivado 2015.2 and implemented on Zynq Board(FPGA).

KEYWORDS : Reconfigurable Johnson counter , LFSR, TPG of Gray counter and Decoder

1 INTRODUCTION

TPG is referred as a Test pattern generation. These test patterns mainly useful for BIST to test digital circuits. Test patterns are generated by number of methods. Some of them are 1.ROM 2.LFSR 3.Binary counters 4. Modified counters 5. LFSR and ROM 6.Cellular automata 7. Exhaustive Pattern generation 8.Weighted Pseudo-Random Pattern generation 9. Pseudo Exhaustive Pattern generation etc

LFSR is Linear feedback shift Register is commonly used as a test pattern generation for BIST (Built in self test) [5] .As a LFSR can built with little area and used not only as a TPG to provides high fault coverage for large scale circuits but also an an Output response Analyzer.[5].A significant correlation exists between the subsequent Test vectors when it is applied to a circuit during its normal operation. The fact is that is to be motivated is several architectural concepts such as cache memories and its central to its effectiveness.In traditional techniques the testing vectors are produced using LFSR [1].There is a limitation of generation of test vectors causes lot of switching operation between subsequent test vectors. There is frequent change over increases Power . P. Girad performed a survey on when there is a frequent change power also increases due to this switching[2], on various internal and external testing.

Earlier days when they need to test digital circuits ATPG is used . It mainly generates the test patterns but it consumes longer time for testing and high cost as it is external testing then there is shift from external testing to internal testing. In internal testing is performed with help of BIST. It manly reduces complex and difficult for testing the circuits The test vectors generated are applied to digital circuits and circuit response obtained compares with its true response to determine the fault.

2. EXISTING METHOD

The existing method mainly consists of producing the test vectors. The vectors were produced by performing the Ex-or operation between Reconfigurable Johnson counter and seed vector.

A. Pattern generation

It mainly includes the generation of test patterns by using the seed vector and Johnson vector .Reconfigurable Johnson counter mainly generates the Johnson vectors and LFSR generates the seed vectors .By doing the EX-OR operation both seed vectors and Johnson vectors produces required test pattern generation.

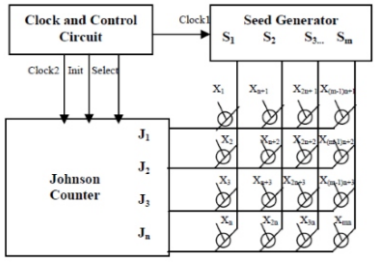

Fig 1 TPG using Reconfigurable Johnson counter and LFSR

B. Generation of Johnson counter

The Johnson vectors were produced by utilizing Reconfigurable Johnson counter. Reconfigurable Johnson counter is constructed with the help of an AND gate, multiplexer and 8 delay flip-flops are connected together to store the bits. Reconfigurable Johnson Counter can operate in three modes.

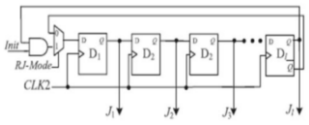

Fig 2 Reconfigurable Johnson counter

Initialization:

When RJ_ Mode is set to 1 and Init is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l time.

Circular shift register mode:

When RJ_ Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 L-times.

Normal mode:

When RJ_Mode is set to logic 0, there configurable Johnson counter will generate 2l unique vectors by clocking CLK2 2L times.

C. LFSR Linear feedback shift Register

In existing method LFSR is used for generation of seed vector .As it is 8 bit LFSR there are 8 D flip-flops which are connected together. D6 and D7 flip-flops outputs are ex-or operation and output it is given as feedback to the input D0 flipflop .

3 PROPOSED METHOD

In this proposed method includes 3bit Gray counter, 3X8 Decoder, Two 8bit registers and adder circuit. The drawback of existing method lack of correlation between subsequent test vectors ,area is overcome by this proposed method .Area is optimized by reducing total gate count with proposed method compared to existing method. The gray counter inputs are Clock and reset .As counter is 3bit so it counts from 000 to 111,and then it repeats .the counter outputs are applied to 3x8 decoder mainly decodes the input e.g. 000 as its input so output is 00000001so the decoder outputs from 00000001 to 10000000 and 8bit register are mainly stores the values of outputs of decoder and now then adder inputs are register 1 and register 2 which mainly adds the two registers values and produce the desired test pattern generation. The patterns produced were applied to Multiplier circuit. The response obtained is compared with the forecasted result to verify the exact functioning of the circuit.

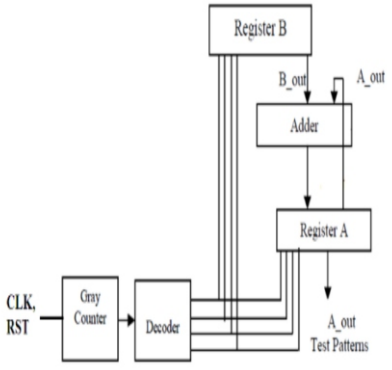

Fig 3 TPG using counter and Decoder

4. TEST RESULTS

A.Simulation result of TPG using Reconfigurable Johnson counter and LFSR

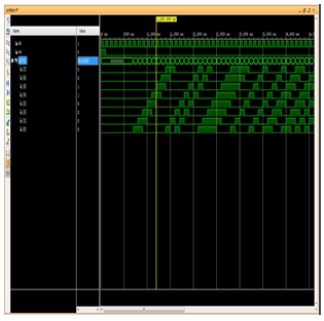

Fig 4. Simulation result of TPG using Reconfigurable Johnson counter and LFSR

B. Schematic diagram of TPG using Gray counter and Decoder.

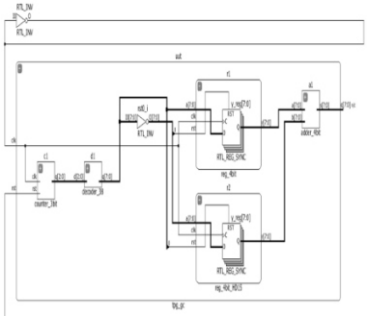

Fig 5 Schematic diagram of TPG using Gray counter and Decoder.

C. Simulation result of TPG using Gray counter and Decoder.

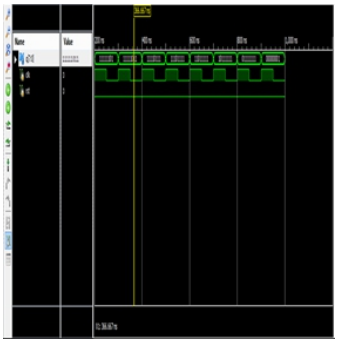

Fig 6 Simulation result of TPG using Gray counter and Decoder

D .Area utilization Report of TPG using gray counter

Slice LUT=71,SliceRegisters =39,
IO =18,clocking =1.
So Total gate count for proposed method is 142
Total gate count for existing method is 185

5 HARDWARE IMPLEMENTATION

Fig 7 Hardware implementation of tpg using Gray counter Hardware : ZYNC board,Device XC7Z020

6 ADVANTAGES

1.The proposed method gives the better area reduction compared to the existing system.
2 Easy to test for the faults.
3.Very little hardware architecture is needed.

7 APPLICATIONS

1.The generated TPG are very useful for BIST
2.Error detecton and Testing.

8 CONCLUSION

The proposed method TPG using gray counter and decoder area reduction i.e 30% compared to existing method TPG using Reconfigurable Johnson counter and LFSR. The test patterns which are generated by Linear feedback shift register and is lack of correlation between the subsequent test patterns is also achieved by the TPG using gray counter and decoder.

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